APPA2.02 SGW111X BLE Module RF Design and PCB Layout Guideline

June 2020 V1.0

Introduction

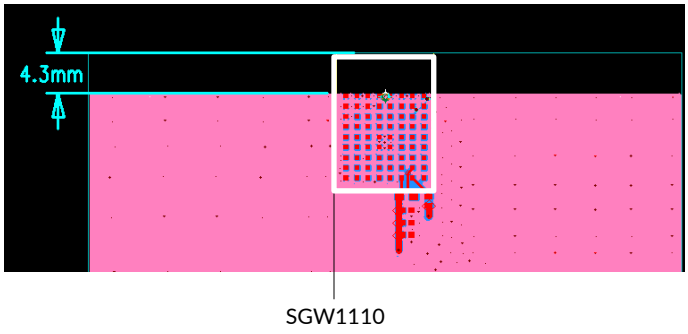
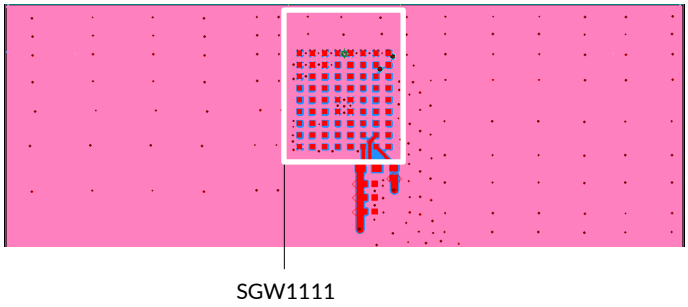
Created for designers, this document provides recommendations for the implementation of layout drawings for the SGW111X BLE Module to reduce noise and optimize circuit performance.

General PCB Layout Techniques

Both four-layer and two-layer FR4 PCB material are recommended for the design, with the former providing an additional advantage of sandwiching between two ground layers the distributed RF decoupling of DC power trace/plane and signal bus, reducing the noise level and unwanted electromagnetic signals.

The layers of the main PCB for both designs are outlined in Table 1.

Antenna Cutout Clearance

SGW1110 BLE Module	SGW1111 BLE Module
Maximum radiated pattern is achieved with a clear cut out for the embedded antenna. The Module should be placed at the center edge of the product main PCBA, with the ground plane cut 4.3mm from the edge to the first pads of the Module for all layer stack. 	Antenna cutout clearance is not required – having the ground plane under the Module is sufficient. 

Filter and Noise Reduction

The SGW111X BLE Module requires a reliable power supply to function properly. Optimal power supply characteristics can be ensured by applying filtering and noise reduction techniques to the host PCB.

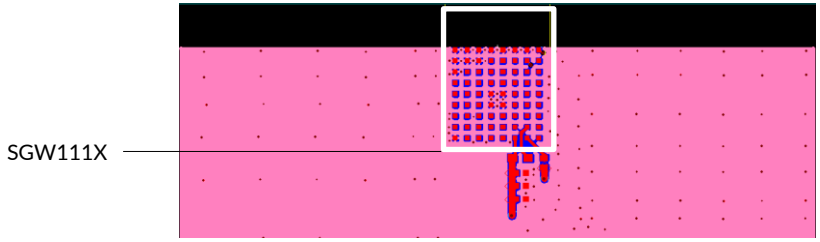
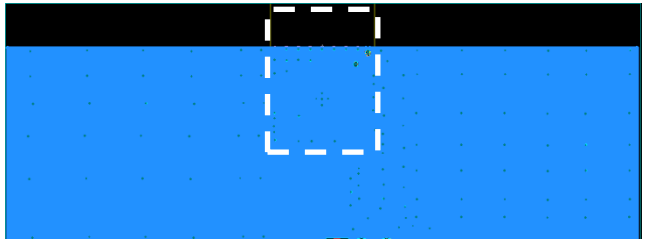
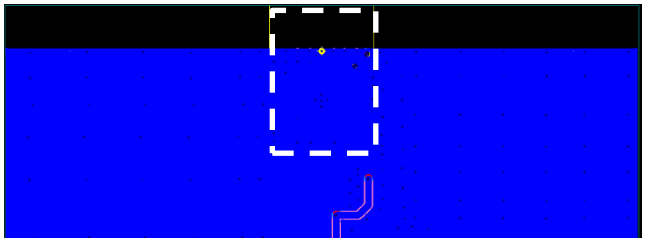
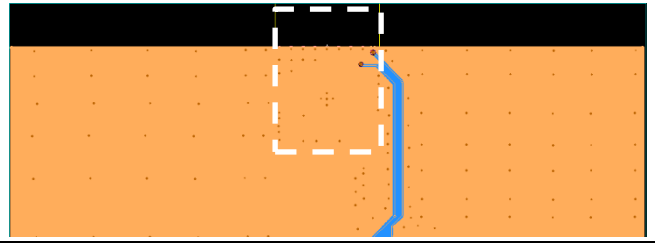
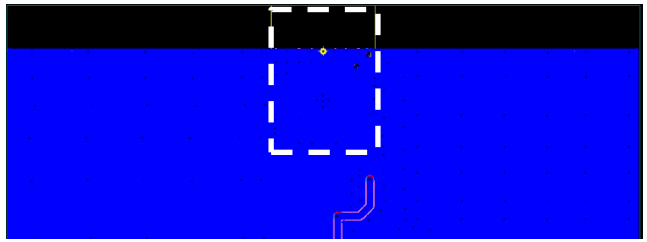
Filter Capacitor

A filter capacitor eliminates noise (low frequency) from the power supply section. It should be physically close to the regulator chip and the recommended value is a minimum of 10uF.

Decoupling Capacitor

Critical for noise reduction, a decoupling capacitor provides a low impedance path for high frequency variations on the power trace. A multi-layer ceramic capacitor is especially effective as it has low ESR and ESL, particularly

Table 1: *Main PCB Layers*

<table>
<tr><th></th><th>Four-layer PCB Design</th><th>Two-layer PCB Design</th></tr>
<tr><td>Layer 1</td><td colspan="2">A ground plane for the Module reduces RF coupling between the Module and DC power circuit or signal bus.
 
</td></tr>
<tr><td>Layer 2</td><td>A reference plane must be built for RF output.
  </td><td rowspan="3">The purposes served by layers 2 to 4 in the four-layer PCB design are combined into one layer in the two-layer PCB design.
  </td></tr>
<tr><td>Layer 3</td><td>Recommended for DC power trace/plane or signal bus routing, the power plane design provides a very low impendence trace at radio frequencies. In addition, the power/signal trace, when surrounded by a ground trace and connected to the reference ground plane, prevents radiated emissions at the board edge.
  </td></tr>
<tr><td>Layer 4</td><td>Recommended for DC power trace/plane or signal bus routing.
  </td></tr>
</table>

with the addition of 47pF, 10nF and 10uF. The capacitor should be placed as close to the Module power input as possible, with the smallest value placed the closest. Applying multiple decoupling capacitors is recommended.

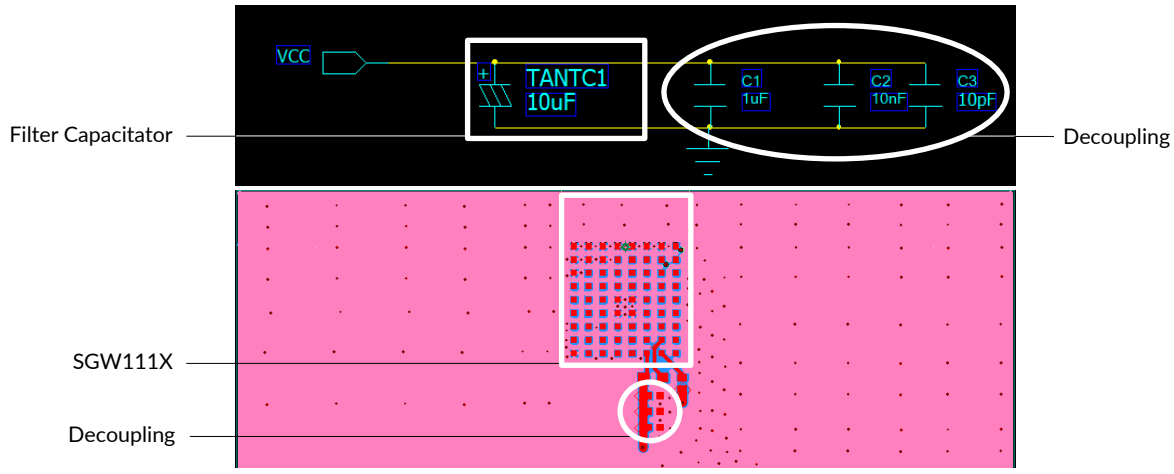


Figure 1: *Decoupling Capacitators on Main PCB*

High Voltage DCDC Switching Supply

To use the high voltage DCDC switching circuit, a 10uH inductor in 0603 package has to be added on the host PCB. The inductor should be placed as close as possible to the Module VCC (Pin 70) and DCCH (Pin 63).

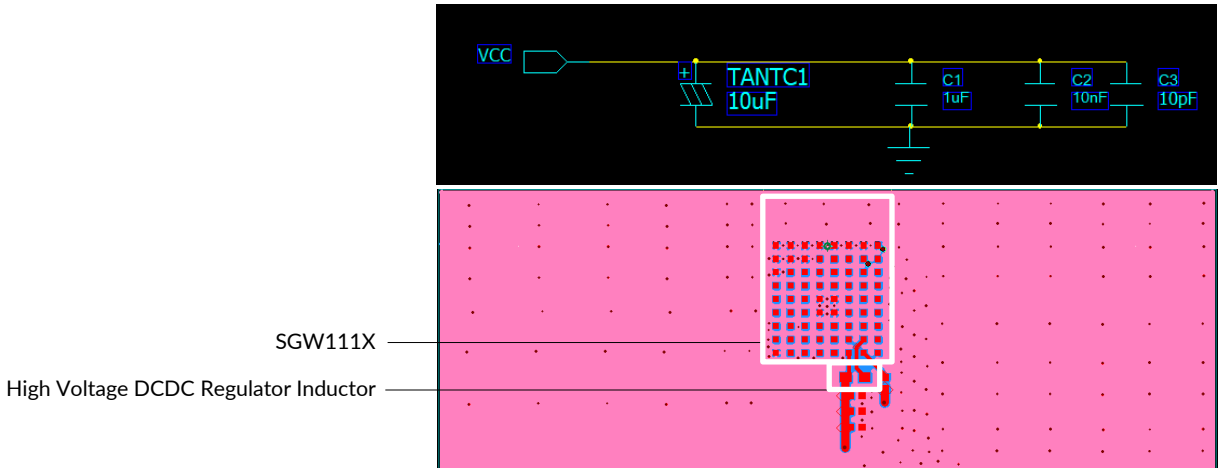


Figure 2: *High Voltage DCDC Switching Supply on Main PCB*

Revision History

Revised	Version	Description
19-Jun-2020	1.0	Initial document release

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