APPA5.02 SGW2828 LoRa Module RF Design and PCB Layout Guideline

June 2020 V1.0

Introduction

Created for designers, this document provides recommendations for the implementation of layout drawings for the SGW2828 LoRa Module to reduce noise and optimize circuit performance.

General PCB Layout Techniques

Both four-layer and two-layer FR4 PCB material are recommended for the design, with the former providing an additional advantage of sandwiching between two ground layers the distributed RF decoupling of DC power trace/plane and signal bus, reducing the noise level and unwanted electromagnetic signals.

The layers of the main PCB for both designs are outlined in Table 1.

50ohm Trace

The RF output must have a surrounding clearance of 0.5mm to prevent RF power loss from the overlapping of the Module RF output pin with the main circuit board ground plane.

The RF trace is kept at 50ohm, but the trace width for the four-layer and two-layer designs differ due to the reference ground plane height. Trace width calculation is outlined below:

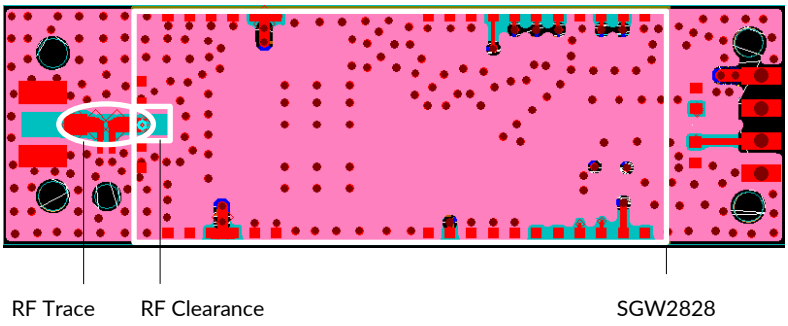


Figure 1: *RF Trace and RF Clearance on Main PCB*

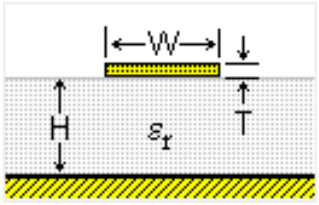
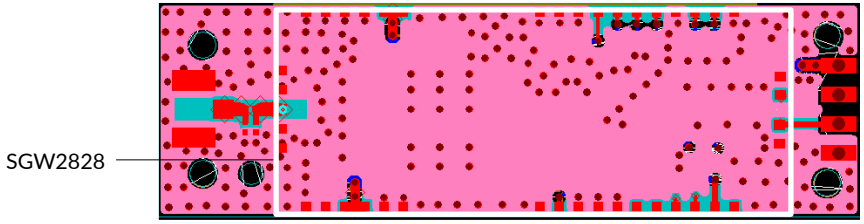
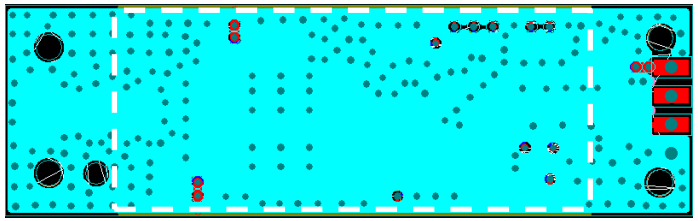
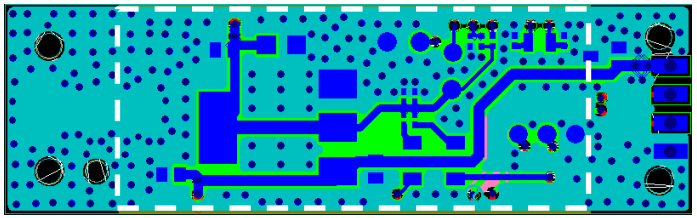
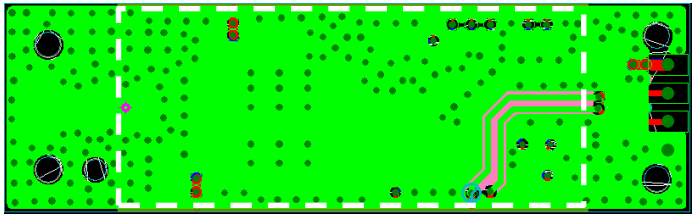
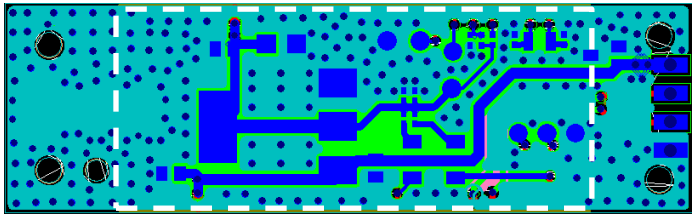
To calculate the required trace width *W*, it is necessary to first figure out the effective dielectric constant e_{eff} as the field generated by the conductor exists partly in air (e = 1) and partly in the dielectric material.	
Assuming that the trace thickness *T* is small compared to the dielectric height (*T/H* < 0.005), e_{eff} can be calculated:	$\left(\frac{W}{H}\right) < 1$: $\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\left(\frac{H}{W}\right)\right)^{-\frac{1}{2}} + 0.04\left(1 - \left(\frac{W}{H}\right)\right)^2\right]$ $\left(\frac{W}{H}\right) > 1$: $\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\left(\frac{H}{W}\right)\right)^{-\frac{1}{2}}$
With e_{eff} calculated, the characteristic impedance of a Microstrip line can be calculated:	$\left(\frac{W}{H}\right) < 1$: $Z_O = \frac{60}{\sqrt{\varepsilon_{eff}}} * \ln\left(8\frac{H}{W} + 0.25\frac{W}{H}\right)$ $\left(\frac{W}{H}\right) > 1$: $Z_O = \frac{\frac{120\pi}{\sqrt{\varepsilon_{eff}}}}{\frac{W}{H} + 1.393 + 0.667\ln\left(\frac{W}{H} + 1.444\right)}$

Table 1: *Main PCB Layers*

<table>
<tr><th></th><th>Four-layer PCB Design</th><th>Two-layer PCB Design</th></tr>
<tr><td>Layer 1</td><td colspan="2">A ground plane for the Module reduces RF coupling between the Module and DC power circuit or signal bus.
 
</td></tr>
<tr><td>Layer 2</td><td>A reference plane must be built for RF output.
  </td><td rowspan="3">The purposes served by layers 2 to 4 in the four-layer PCB design are combined into one layer in the two-layer PCB design.
  </td></tr>
<tr><td>Layer 3</td><td>Recommended for DC power trace/plane or signal bus routing, the power plane design provides a very low impendence trace at radio frequencies. In addition, the power/signal trace, when surrounded by a ground trace and connected to the reference ground plane, prevents radiated emissions at the board edge.
  </td></tr>
<tr><td>Layer 4</td><td>Recommended for DC power trace/plane or signal bus routing.
  </td></tr>
</table>

Crystal 32.768KHz

A ground plane placed under the crystal prevents clock signal coupling to the DC power trace/ plane or signal bus.

If LoRaWAN or sleep mode is needed in the design, TCXO has to be added to the host PCB.

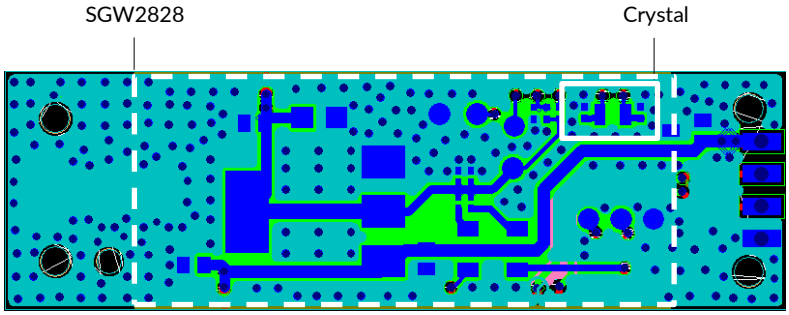


Figure 2: *Crystal on Main PCB*

Filter and Noise Reduction

The SGW2828 LoRa Module requires a reliable power supply to function properly. Optimal power supply characteristics can be ensured by applying filtering and noise reduction techniques to the host PCB.

Filter Capacitor

A filter capacitor eliminates noise (low frequency) from the power supply section. It should be physically close to the regulator chip and the recommended value is a minimum of 10uF.

Decoupling Capacitor

Critical for noise reduction, a decoupling capacitor provides a low impedance path for high frequency variations on the power trace. A multi-layer ceramic capacitor is especially effective as it has low ESR and ESL, particularly with the addition of 47pF, 10nF and 10uF. The capacitor should be placed as close to the Module power input as possible, with the smallest value placed the closest. Applying multiple decoupling capacitors is recommended.

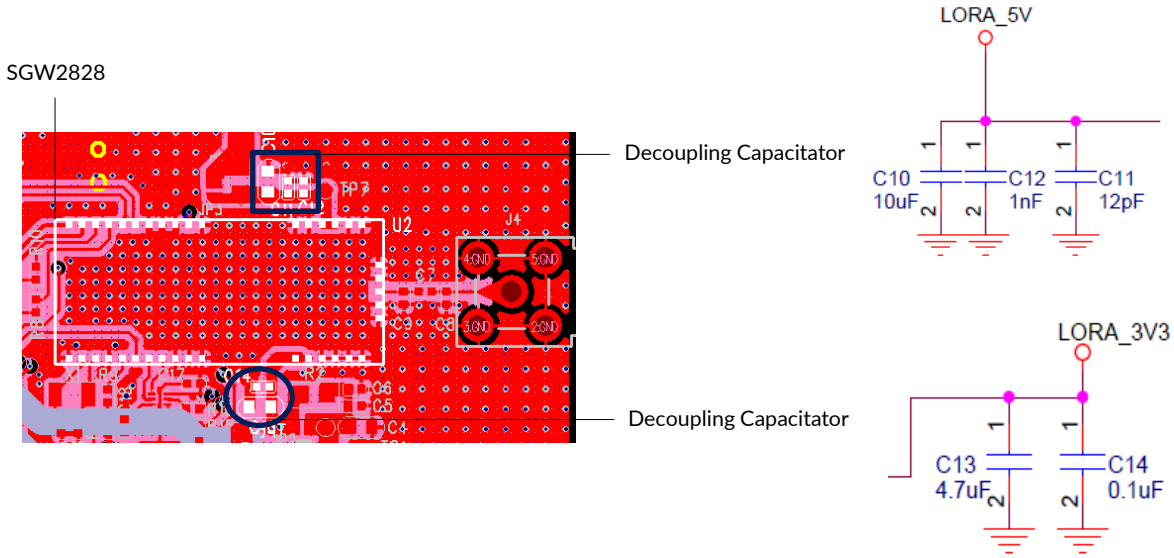


Figure 3: *Decoupling Capacitators on Main PCB*

Optimization

An antenna matching network can ensure that the antenna is matched to 50ohm networks. A matched network allows maximum RF output power.

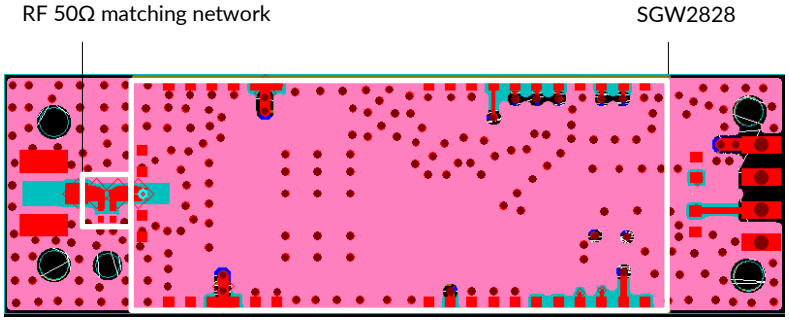


Figure 4: *Antenna Matching Network on Main PCB*

Revision History

Revised	Version	Description
18-Jun-2020	1.0	Initial document release

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